AMENDMENTS TO THE CLAIMS

Claims 1-23 (canceled)

Claim 24 (Newly Added): A circuit arrangement comprising:

a flip-flop having a plurality of storage transistors with a threshold voltage of a first value;

a first power switch transistor having a threshold voltage of a second value, wherein an application of a predetermined electrical potential to the first power switch transistor's gate terminal brings the circuit arrangement to an operating state in which if at least one supply voltage is switched off, electric charge carriers contained in the circuit arrangement are prevented from discharging from the circuit arrangement; and

a plurality of switching transistors, having a threshold voltage of a third value, provided between the flip-flop and the first power switch transistor, for coupling a flip-flop input signal into the flip-flop;

wherein the magnitude of the first and/or the second value is greater than the magnitude of the third value.

Claim 25 (Newly Added): The circuit arrangement according to Claim 24, wherein the flip-flop has two inverters formed from the storage transistors.

Claim 26 (Newly Added): The circuit arrangement according to Claim 24, wherein the first power switch transistor is a common power switch transistor provided for the flip-flop and for at least one additional flip-flop.

Claim 27 (Newly Added): The circuit arrangement according to one of Claim 24, wherein the thickness of a gate insulating layer of the storage transistors and/or of the first power switch transistor is greater than the thickness of the gate insulating layer of the switching transistors.

Claim 28 (Newly Added): The circuit arrangement according to Claim 24, wherein a channel width of the storage transistors and/or of the first power switch transistor is less than the channel width of the switching transistors.

Claim 29 (Newly Added): The circuit arrangement according to Claim 24, wherein the switching transistors are connected such that, in an operating state of the circuit arrangement in which at least one supply voltage of the circuit arrangement is switched off, each of the terminals of the switching transistors has a defined electrical potential.

Claim 30 (Newly Added): The circuit arrangement according to Claim 24, having at least one second power switch transistor, which is coupled to at least a portion of the switching transistors such that, in an operating state of the circuit arrangement in which at least one supply voltage of the circuit arrangement is switched off, a gate terminal of each of the switching transistors coupled to the at least one second power switch transistor has a defined electrical potential.

Claim 31 (Newly Added): The circuit arrangement according to Claim 24, having at least one third power switch transistor, which is coupled to at least a portion of the switching transistors such that,

in an operating state of the circuit arrangement in which at least one supply voltage of the circuit arrangement is switched off, a source/drain terminal of each of the switching transistors coupled to the at least one third power switch transistor has a defined electrical potential.

Claim 32 (Newly Added): The circuit arrangement according to Claim 31, wherein the at least one third power switch transistor is a p-MOS field effect transistor.

Claim 33 (Newly Added): The circuit arrangement according to Claim 24, further comprising a pulse generator circuit that generates a flip-flop input signal from an input signal and from a clock signal and is coupled to the first power switch transistor and to the switching transistors.

Claim 34 (Newly Added): The circuit arrangement according to Claim 33, wherein the pulse generator circuit comprises a plurality of pulse generator transistors having a threshold voltage of a fourth value, wherein the magnitude of the first and/or the second value is greater than the magnitude of the fourth value.

Claim 35 (Newly Added): The circuit arrangement according to Claim 33, wherein the pulse generator circuit comprises a logic subcircuit that generates at least one flip-flop input signal from at least one input signal in accordance with a predetermined logic operation.

Claim 36 (Newly Added): The circuit arrangement according to Claim 35, wherein the logic subcircuit operates as one of an inverter, AND gate, OR gate, NAND gate, NOR gate, exclusive OR gate, and exclusive NOR gate.

Claim 37 (Newly Added): The circuit arrangement according to Claim 36, wherein the logic subcircuit comprises a plurality of logic transistors having a threshold voltage of a fifth value, wherein the magnitude of the first and/or the second value is greater than the magnitude of the fifth value.

Claim 38 (Newly Added): The circuit arrangement according to Claim 24, further comprising a control unit that controls supply voltages applied to terminals of at least a portion of the transistors of the circuit arrangement, wherein the control unit is set such that, in an energy saving operating state, the control unit can switch off all the supply voltages except for supply voltages of the flip-flop.

Claim 39 (Newly Added): The circuit arrangement according to Claim 24, further comprising a test circuit coupled to the flip-flop, wherein the test circuit tests functionality of the flip-flop.

Claim 40 (Newly Added): The circuit arrangement according to Claim 39, wherein the test circuit has an input component that programs a test input signal of the flip-flop, and an output component that reads a test output signal of the flip-flop.

Claim 41 (Newly Added): The circuit arrangement according to Claim 39, wherein the test circuit has a plurality of test transistors with a threshold voltage having a sixth value, wherein the magnitude of the sixth value is greater than at least one of the magnitudes of the third to fifth values.

Claim 42 (Newly Added): The circuit arrangement according to Claim 41, wherein the test transistors have a gate insulating layer having a thickness greater than a thickness of the gate insulating layer of the switching transistors.

Claim 43 (Newly Added): The circuit arrangement according to Claim 34, wherein the test transistors have a gate insulating layer having a thickness greater than a thickness of a gate insulating layer of the pulse generator transistors.

Claim 44 (Newly Added): The circuit arrangement according to Claim 37, wherein the test transistors have a gate insulating layer having a thickness greater than a thickness of a gate insulating layer of the logic transistors.

Claim 45 (Newly Added): The circuit arrangement according to Claim 24, further comprising one or more protection transistors having a threshold voltage of a seventh value and located between the flip-flop and the switching transistors, wherein the protection transistors selectively couple or decouple the flip-flop and the switching transistors, and the magnitude of the seventh value is greater than the magnitude of the third value.

Claim 46 (Newly Added): The circuit arrangement according to Claim 45, wherein the protection transistors have a gate insulating layer having a thickness greater than a thickness of the gate insulating layer of the switching transistors.

Claim 47 (Newly Added): The circuit arrangement according to Claim 34, further comprising one or more protection transistors having a threshold voltage of a seventh value and located between the flip-flop and the switching transistors, wherein the protection transistors selectively couple or decouple the flip-flop and the switching transistors, and the magnitude of the seventh value is greater than the magnitude of the third value, and

wherein the protection transistors have a gate insulating layer having a thickness greater than a thickness of the gate insulating layer of the pulse generator transistors.

Claim 48 (Newly Added): The circuit arrangement according to Claim 37, further comprising one or more protection transistors having a threshold voltage of a seventh value and located between the flip-flop and the switching transistors, wherein the protection transistors selectively couple or decouple the flip-flop and the switching transistors, and the magnitude of the seventh value is greater than the magnitude of the third value, and

wherein the protection transistors have a gate insulating layer having a thickness greater than the thickness of a gate insulating layer of the logic transistors.

Claim 49 (Newly Added): The circuit arrangement according to Claim 45, wherein

in a first operating state, when at least one supply voltage of the circuit arrangement is switched off, by applying electrical control signals to at least a portion of the protection transistors, the protection transistors electrically decouple the flip-flop and the switching transistors from one another; and

in a second operating state, when supply voltages are applied to the circuit arrangement, by applying electrical control signals to at least a portion of the switching transistors, the switching transistors electrically couple the flip-flop and the switching transistors to one another.

Claim 50 (Newly Added): The circuit arrangement according to Claim 45, wherein the protection transistors have at least one transistor pair of transistors of different conduction types connected in parallel with one another, and at least one transistor pair connected by its source/drain terminals between the flip-flop and the switching transistors.